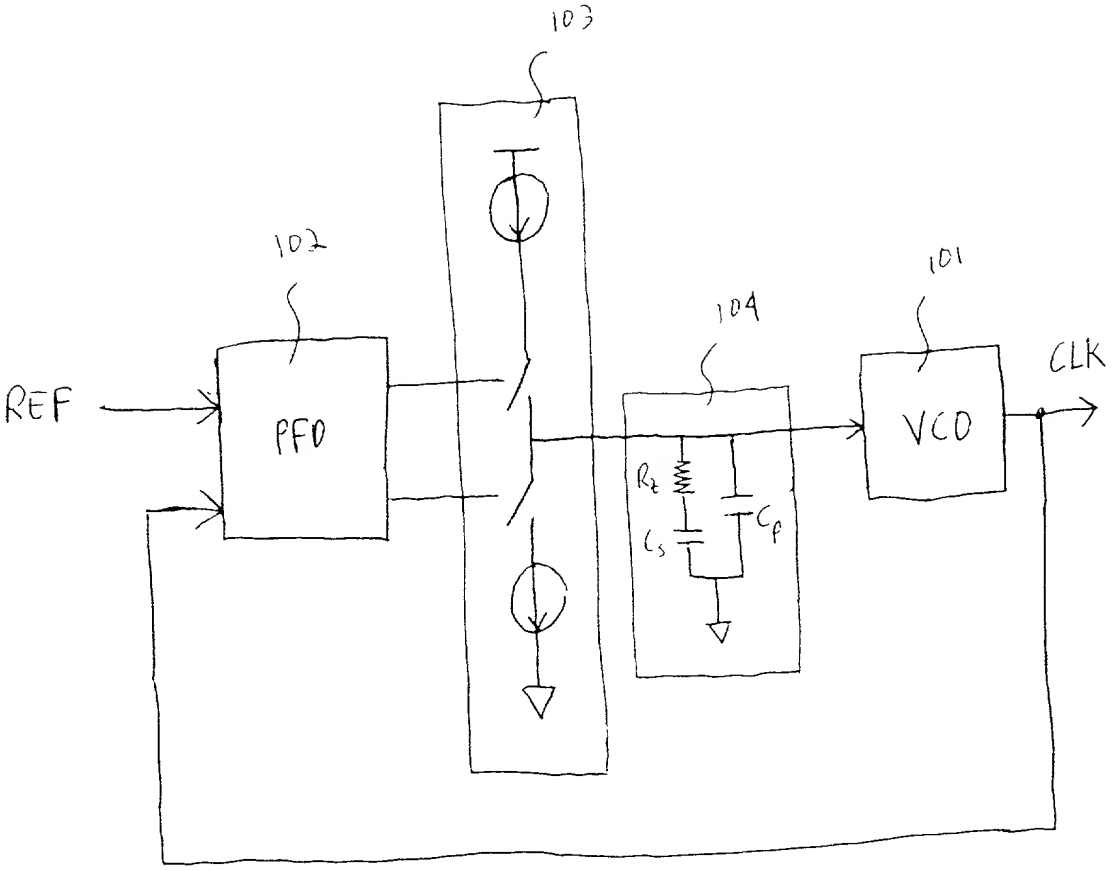


FIG. 1

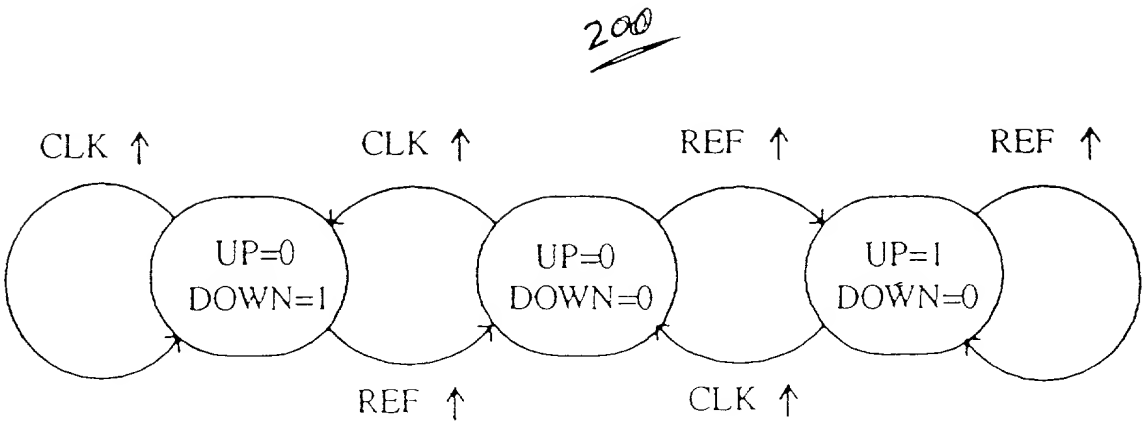


Fig. 2. PFD State Diagram

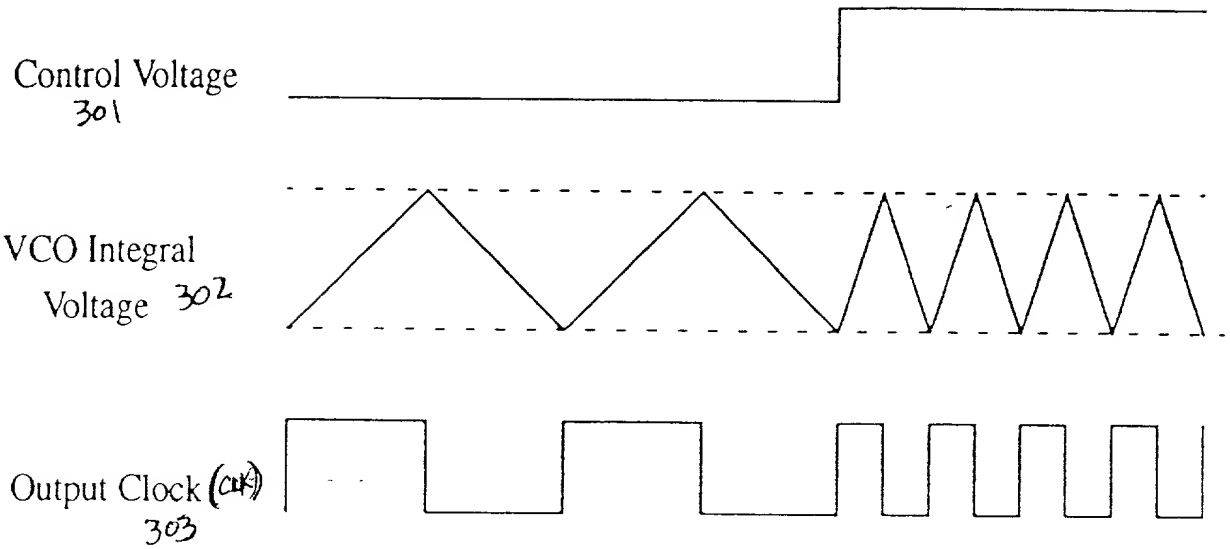


Fig. 3. VCO operation

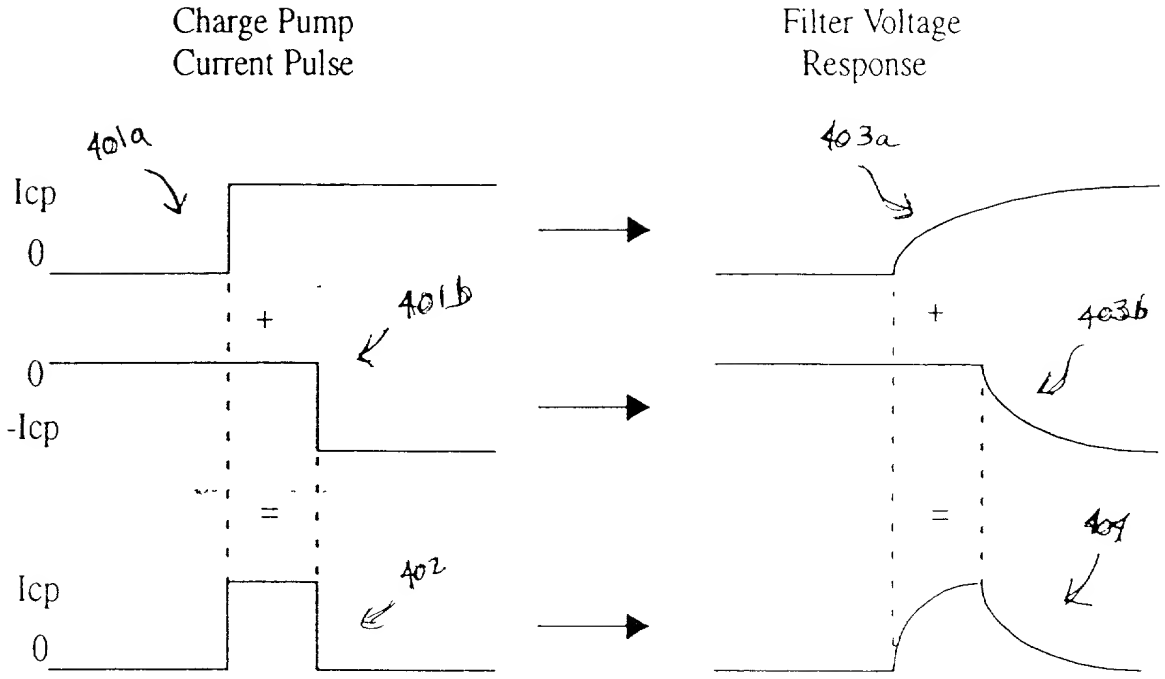


Fig. 4 Charge-Pump/Filter Model

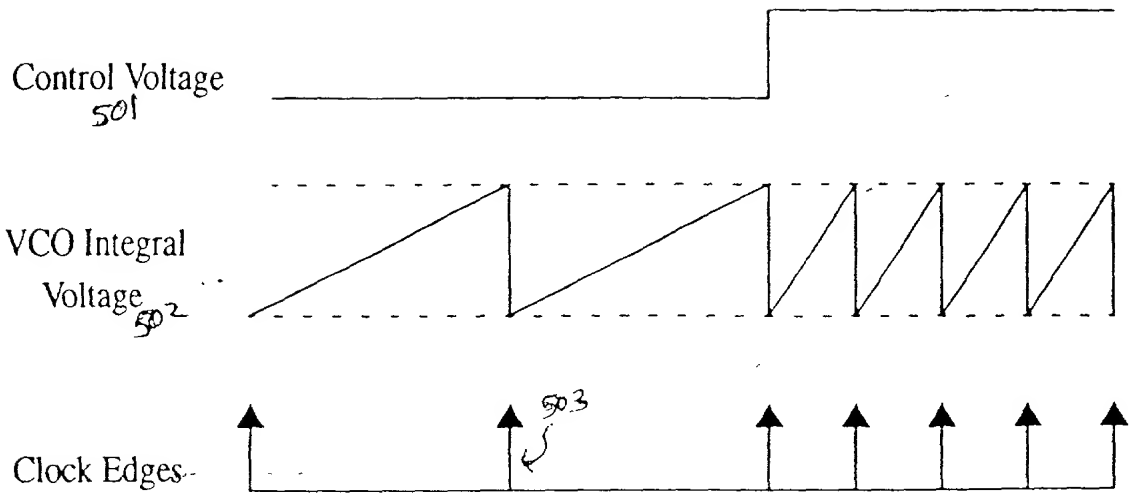


Fig. 5. Mathematical Representation of the VCO

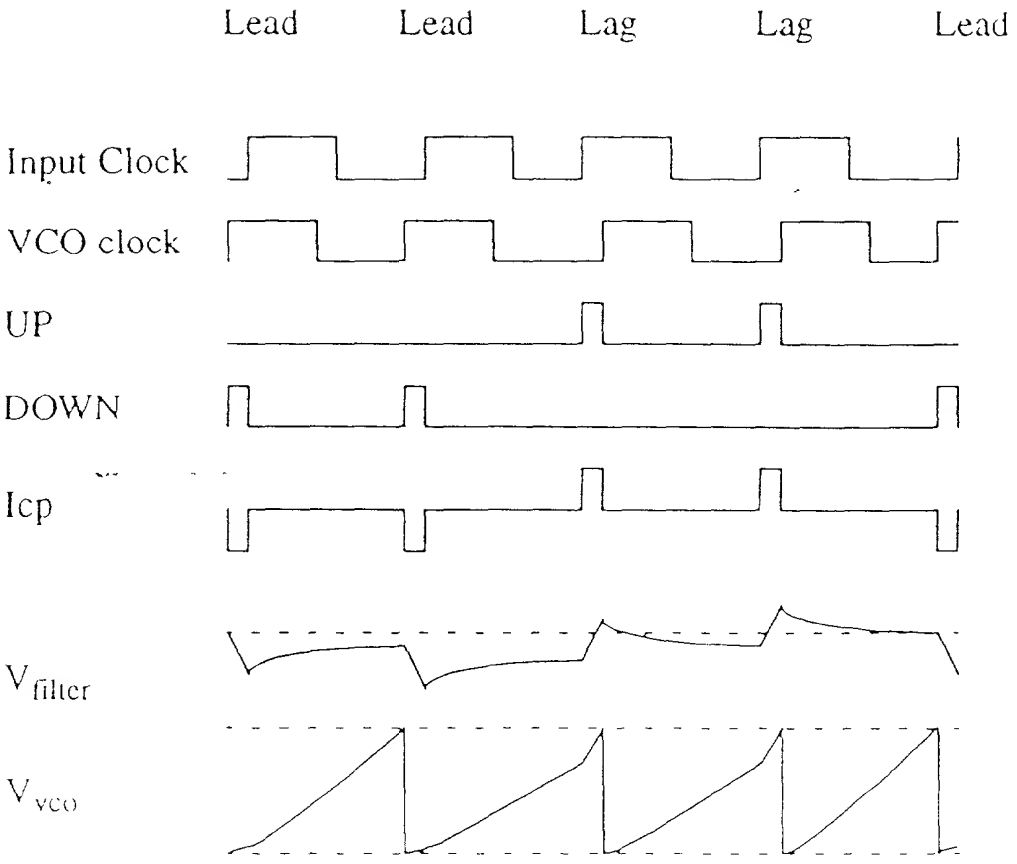
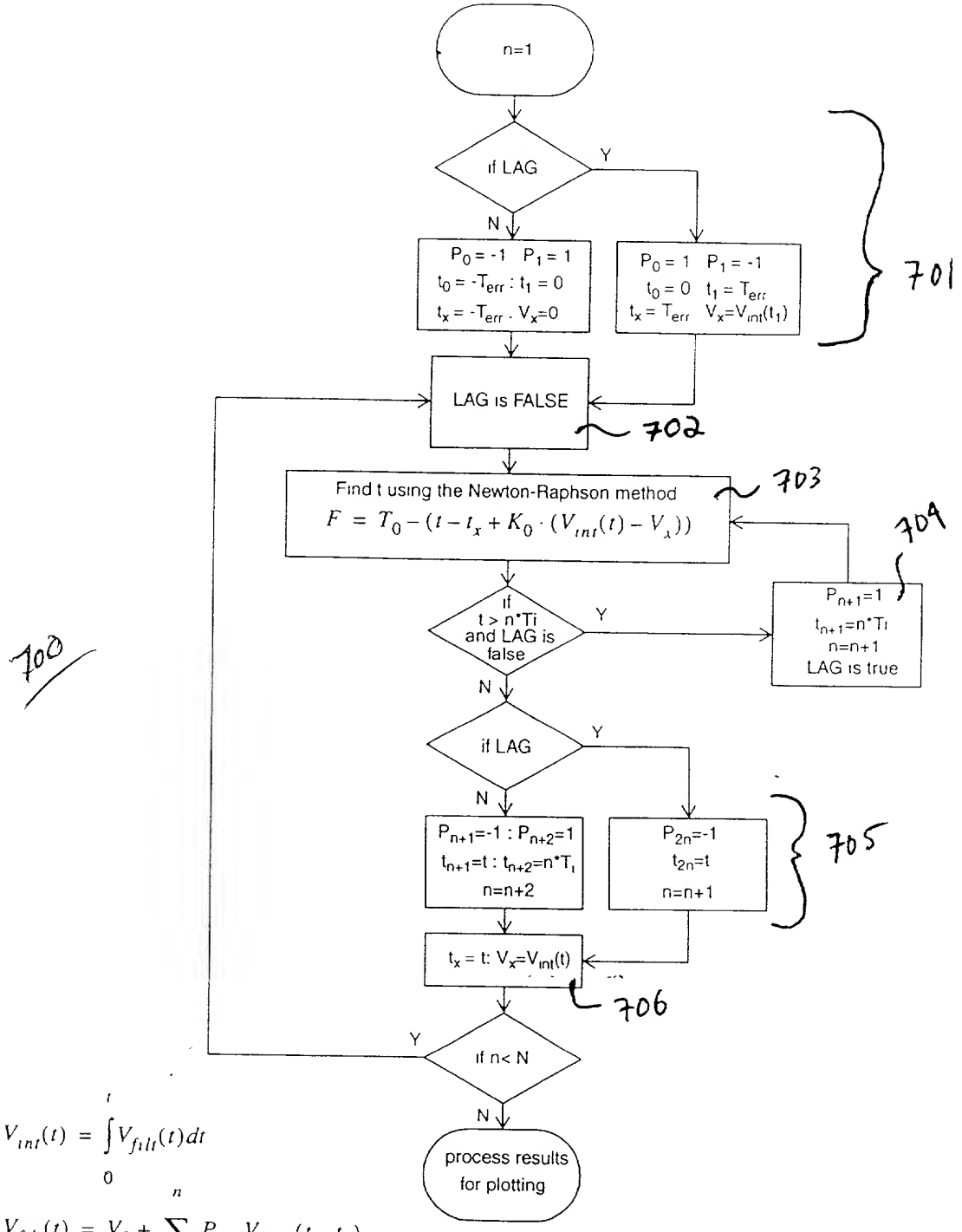


Fig. 6. PLL Operation



$$V_{int}(t) = \int_0^t V_{filt}(t)dt$$

$$V_{filt}(t) = V_0 + \sum_{k=1}^{n} P_k \; V_{step}(t - t_k)$$

Fig. 7. Model Flowchart

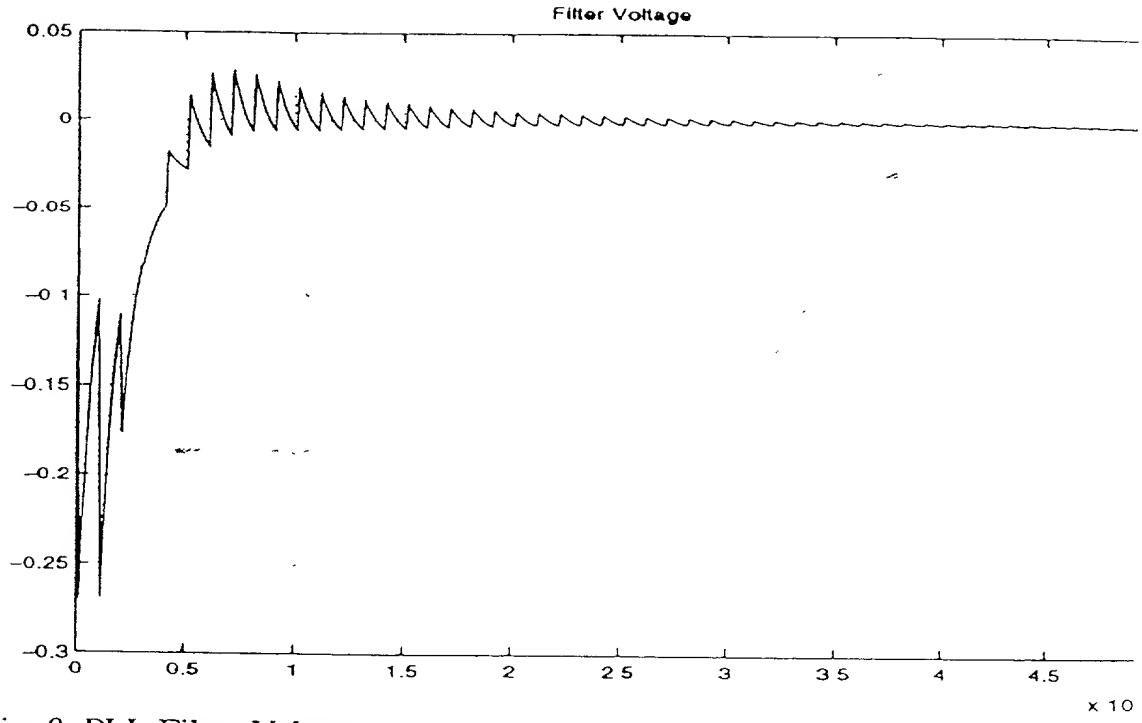


Fig. 8. PLL Filter Voltage

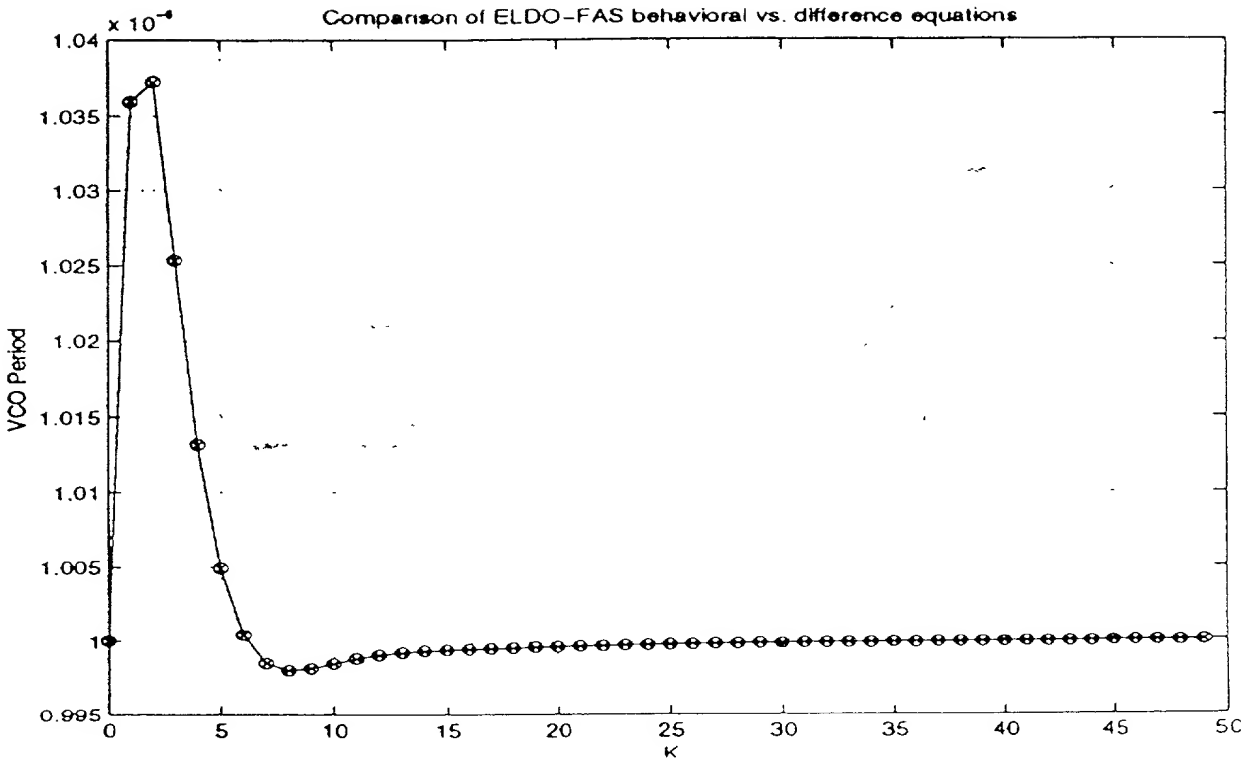


Fig. 9. PLL Output Clock Period

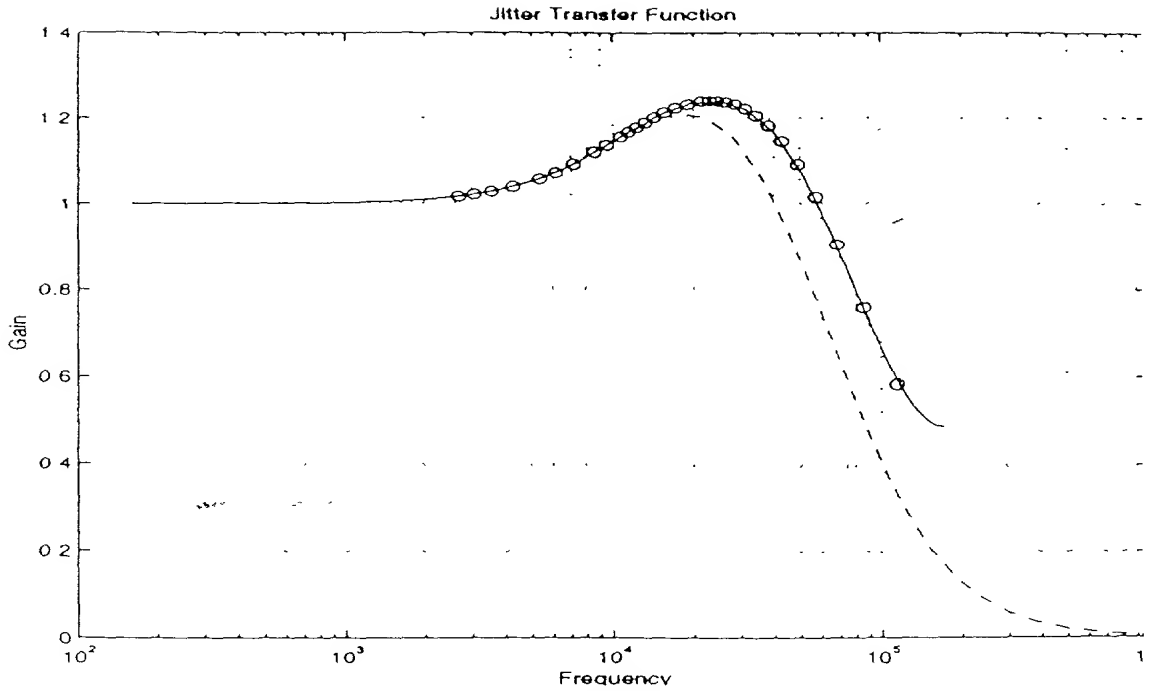


Fig. 10. Bode Plot of Jitter Transfer Function

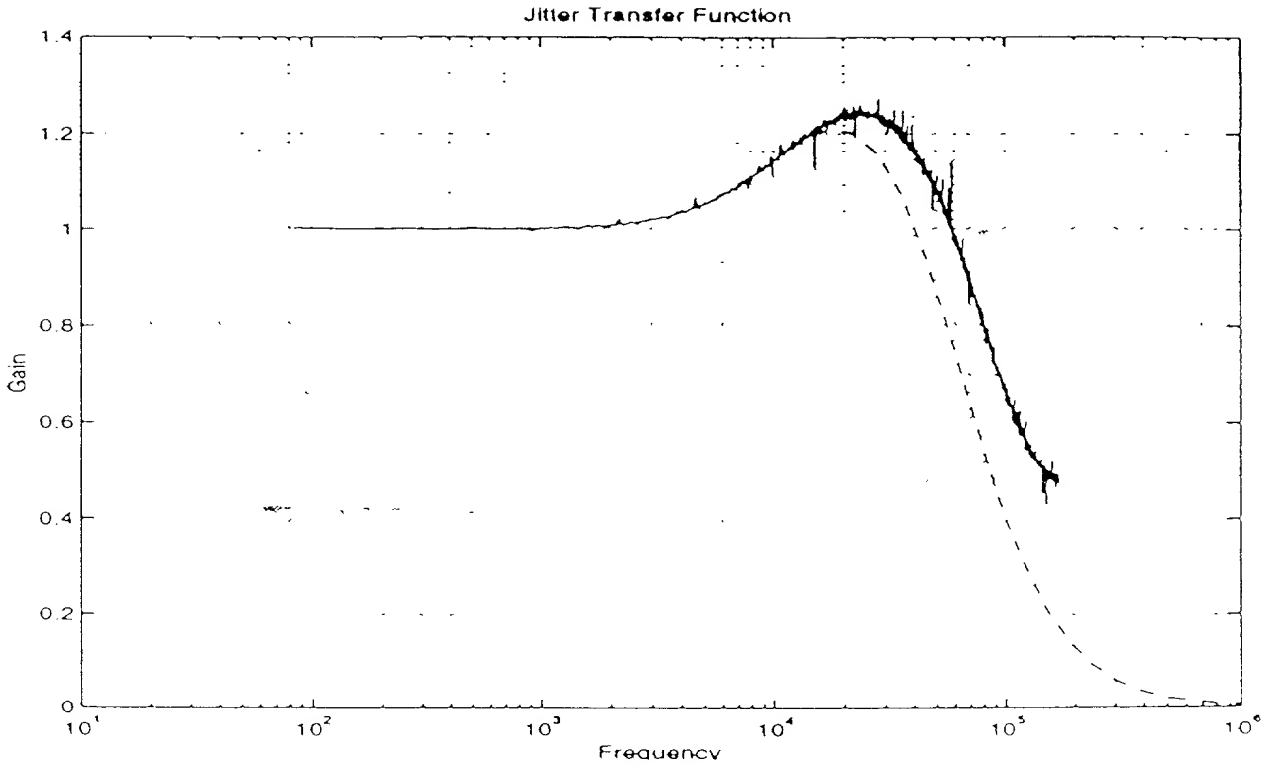


Fig. 11. Bode Plot of Jitter Transfer Function

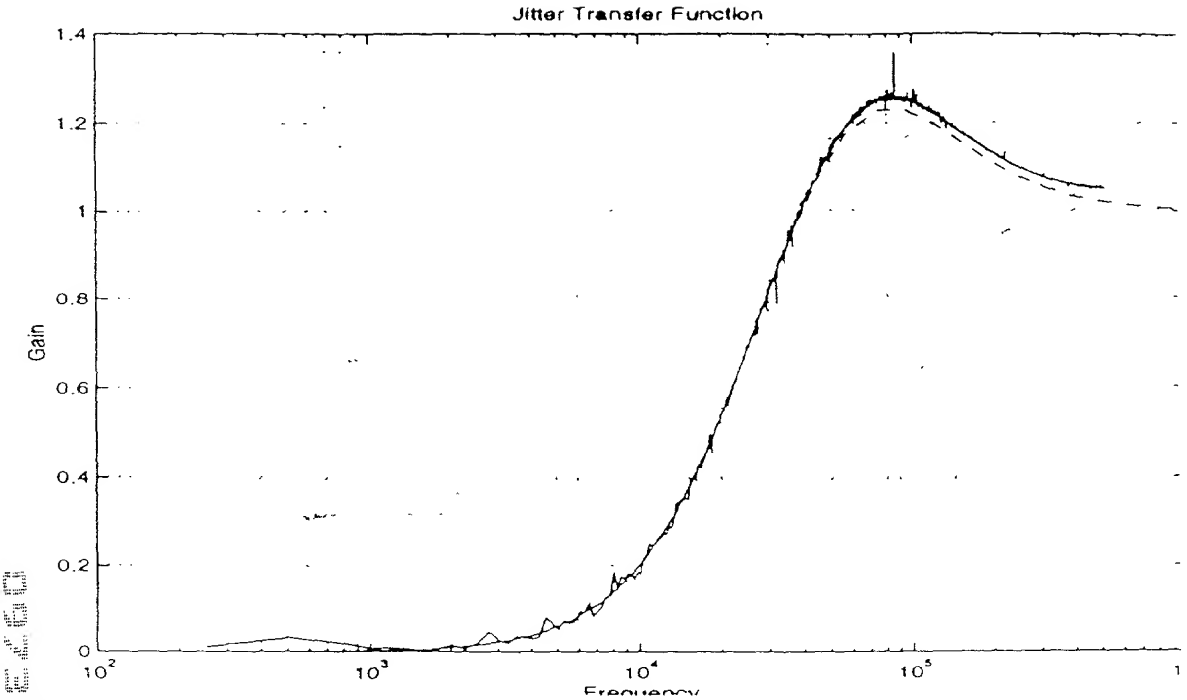
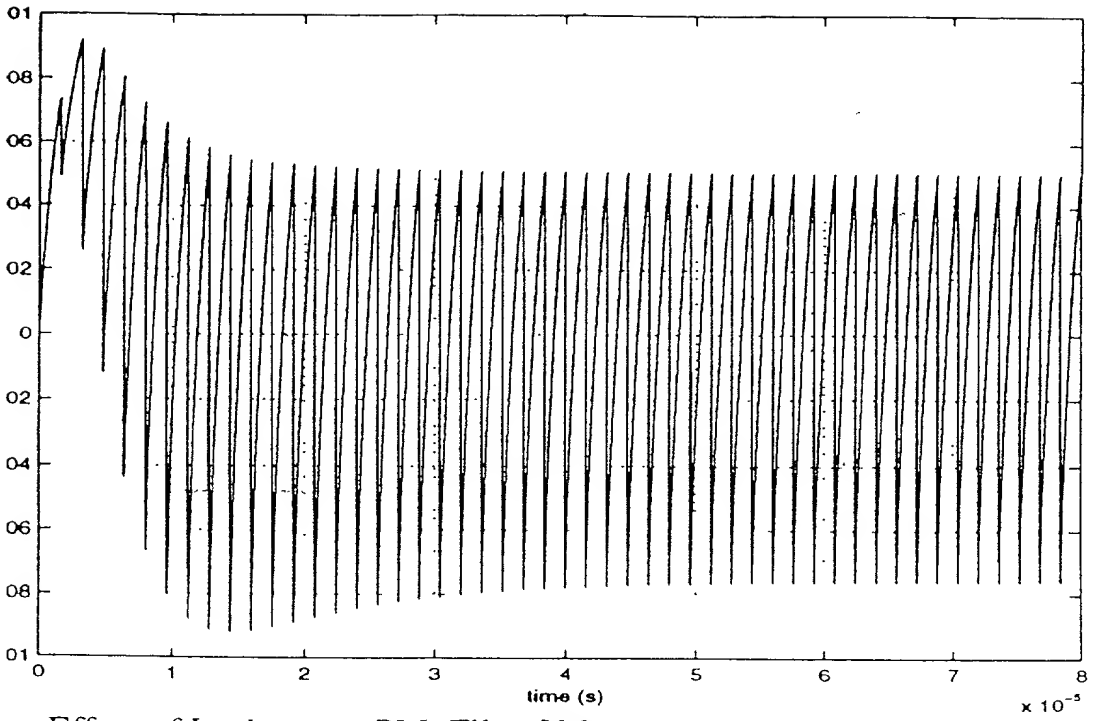


Fig. 12. Bode plot of VCO Transfer Function



Effect of Leakage on PLL Filter Voltage

FIGURE 13

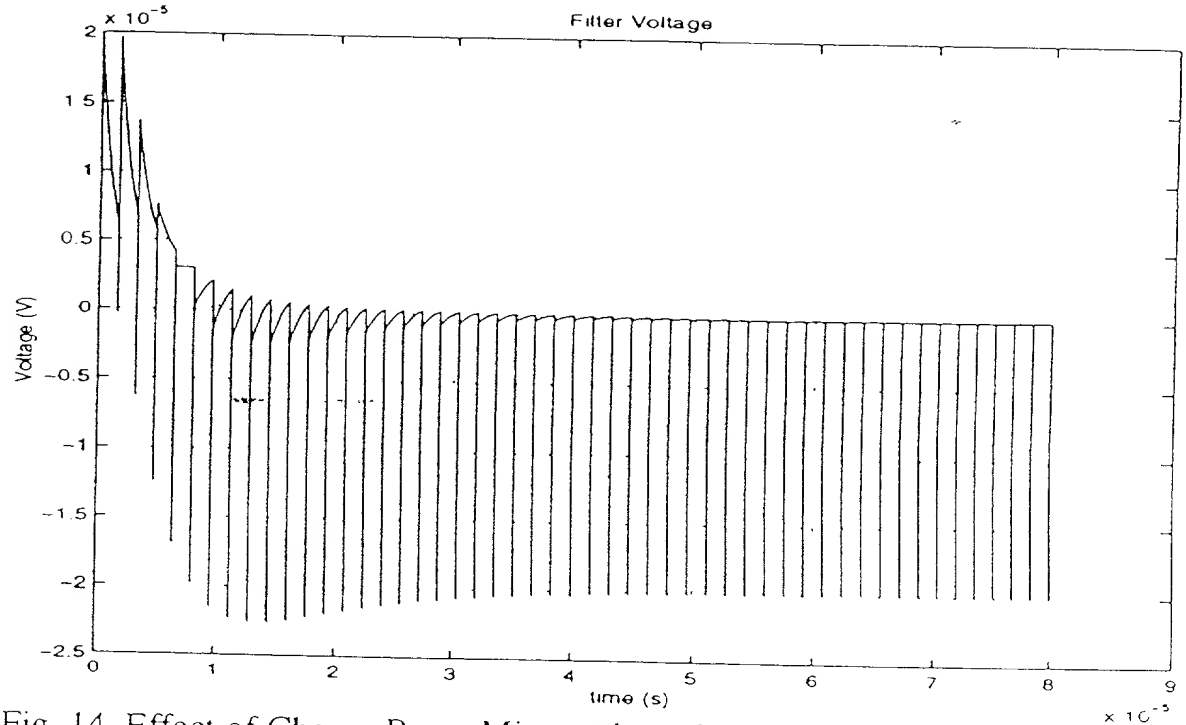


Fig. 14. Effect of Charge-Pump Mismatch on PLL Filter Voltage